Spiking Neural Networks based Rate-Coded Logic Gates for Automotive Applications in BiCMOS

Hendrik M. Lehmann, Julian Hille, Cyprian Grassmann, Vadim Issakov

***Abstract*—Spiking Neural Networks (SNNs) represent the third generation of artificial neural networks. In this work, we evaluate the core element of SNN, the neuron circuit equivalent, in terms of temperature robustness for automotive applications. Thanks to the operating point stabilization, the proposed circuit-level neuron implementation achieves a broad frequency tuning range up to 42 MHz and operates over a wide temperature range from −40 °C to 125 °C. At the maximum spiking frequency of 42 MHz, the circuit consumes a DC power of only 300 nW. We use the proposed neuron circuit to realize two fundamental logic gates, AND and OR, by means of analog rate-encoded spiking neural networks. To the best of the authors' knowledge, these are the first reported SNN-based logic gates measured over the automotive temperature range. We showcase the suitability of SNN circuit implementation for automotive applications. The circuits are realized in a 130 nm BiCMOS.**

I. Introduction

ARTIFICIAL Neural Networks (ANNs) is an emerging, highly relevant research field nowadays. In particular, the third generation of ANNs, the Spiking Neural Networks (SNNs) are gaining major attention, as they are inspired by their biological counterparts and often attempt to achieve biological plausibility in neuroscience [1], [2]. In many applications, they seem to be a promising approach, e.g. for pattern recognition [3]. However, the exact biological plausibility of a circuit-level neuron emulation is often less important for technical applications, but rather its reducibility to necessary neuron functions as well as the applicability to respond properly in specific cases. In many cases, it is sufficient that the circuit-level neuron equivalent is able to mimic only some less complex spiking patterns (e.g. regular and fast spiking), unlike its biological original, which generates many more additional patterns (e.g. bursting, chattering, thalamo-cortical spikes) [4].

Most applications are software-driven. Completely analog SNN implementations, which perform highly complex tasks, have not been reported yet. Almost all implementations so far are related to low frequency applications [5]. Only few works report operation in the radio frequency (RF) domain [6]. Spiking Neural Networks offer more efficient processing and could therefore be used for pattern recognition of radar targets or interferences from the raw radar data. Hence, processing of radar signals after down-conversion into the baseband is a potential use case for neuromorphic circuits [7]. Automotive radar applications pose an additional challenge, as circuits must operate over a wide ambient temperature range of −40 °C - 125 °C [8].

Hendrik M. Lehmann and Vadim Issakov are with Infineon Technologies AG, Neubiberg, Germany and Chair of CMOS Design, TU Braunschweig, Germany. e-mail: Hendrik.Lehmann@infineon.com.

Julian Hille is with Infineon Technologies AG, Neubiberg, Germany, and Chair of Robotics, AI and Real-time Systems, TU Munich, Germany.

Cyprian Grassmann is with Infineon Technologies AG, Neubiberg, Germany.

Publications reporting implementation of logic gates using spiking neural networks mainly deal with the XOR gates [9], [10]. This is related to the fact that the nonlinear properties of such networks offer a promising approach to solve nonlinear separation of XOR gates. However, basic AND and OR gates are also of interest, since they are the basis for most of today's digital circuits. To the best of the authors' knowledge, the implementation of an analog SNN-based solution for AND and OR gates has not yet been reported in the literature yet.

In this work, we investigate the applicability of SNN circuit-level realization for automotive applications. For this purpose, we propose a modified circuit implementation of the Izhikevich neuron model. The proposed modification enables the linear frequency tuning functionality of a neuron. Unlike in the classical Izhikevich neuron, mimicking all possible biologically plausible patterns is not targeted here [11]. By stabilizing the operating point of the circuit, it is intended to achieve a stable behavior over a wide temperature range. Next, we derive simple networks using the realized neuron model to showcase its functionality. Logical AND and OR gates are implemented in a rate-coded SNN architecture and their properties are investigated for the automotive applications.

Numerous millimeter-wave radar transceivers are realized in SiGe BiCMOS technologies [12], [13], as they offer advantages over CMOS processes in terms of flicker noise, RF performance over temperature, reliability and cost [14]. Hence, we realize circuits here in a 130 nm SiGe BiCMOS technology.

II. Neuron Design and Logic Gate Configuration

A. Modified Izhikevich Neuron

The circuit-level neuron implementation used in this work has a similar topology as the one reported in [11]. We propose extending the circuit by an enhanced current mirror. The proposed circuit is shown in Fig. 1.

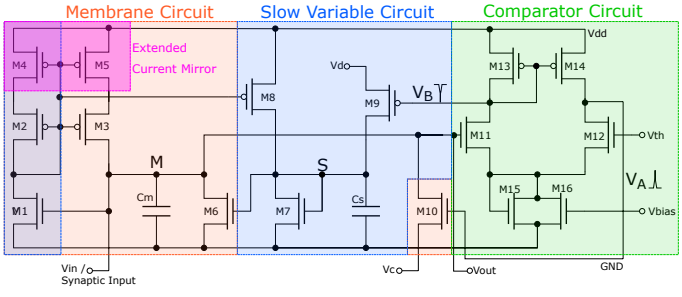

Fig. 1. Schematic of the modified Izhikevich neuron realized in this work.

The authors of the circuit in [11] show an Izhikevich model, which is capable of mimicking biological patterns related to different neuronal activities. Generation of various patterns is based on a instability of the operating point when

different tuning voltages are applied. However, this is often not necessary for most applications. Yet, a wide frequency tuning is more useful, as it allows the circuit to respond to different input signals at different frequencies. Hence, the circuit modification in Fig. 1 enables achieving stability of the operating point even for different tuning voltages. A robust circuit behavior is obtained over a wide temperature range due to the enhanced stability.

The transistor sizes of the circuit shown in Fig. 1 in micrometers are $(W/L)_{M_{1,9,10,11,12}} = (1.4/0.5)$, $(W/L)_{M_{2,4,5,7}} = (2/0.72)$, $(W/L)_{M_3} = (1.4/3)$, $(W/L)_{M_6} = (1.4/7)$, $(W/L)_{M8} = (1.4/5)$, $(W/L)_{M_{13}} = (2/0.5)$, $(W/L)_{M_{14}} = (2.3/0.5)$, $(W/L)_{M_{15,16}} = (1.4/1)$. The capacitance values are $C_m = 17\,\text{fF}$ and $C_s = 45\,\text{fF}$.

Compared to [11], the basic operation of the circuit remains the same and will be briefly explained in the following. The circuit contains a total of 16 transistors and two capacitors C_m and C_s, which are used to represent the two state variables of the membrane voltage (M) and slow variable (S). The circuit can be divided into three sub-circuits: the membrane circuit (M_1 -M_6, M_{10}), the slow variable circuit (M_1, M_2, M_4, M_7 - M_9) and the comparator circuit (M_{11} - M_{16}). In the membrane potential circuit, a synaptic input current is integrated via the capacitor C_m, as well as additional internal currents, which depend on the state of the circuit. In contrast to the previously described circuits, the current mirror is extended by two additional transistors (M_4, M_5) in order to ensure a stable operating point. The slow variable circuit with the capacitor C_s works similarly, integrating the currents that are in relation to M and S. The comparator circuit is used for the spike generation and creates the pulses (V_a and V_b), which cause a spike reset of the circuit. The tuning variables V_c and V_d control the reset mechanism and can be used to enhance the neuron's frequency sensitivity.

Fig. 2 shows the general functionality of the neuron. If a sufficiently large input impulse is provided, the neuron generates an output spike. This corresponds to the biological behaviour of a regular spiking neuron. The input pulse has an amplitude of $V_{in} = 400\,\text{mV}$ and a pulse width of $\tau_{in} = 160\,\text{ns}$, the tuning variables are set to $V_c = 200\,\text{mV}$ and $V_d = 400\,\text{mV}$. The bias voltage and threshold voltages are $V_{bias} = 20\,\text{mV}$ and $V_{th} = 250\,\text{mV}$. The supply voltage is $V_{dd} = 1.5\,\text{V}$.

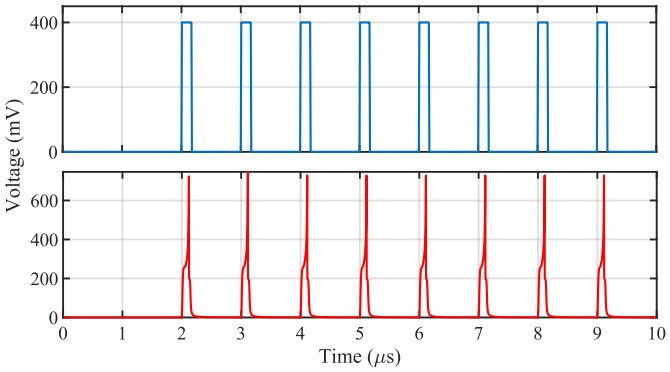

Fig. 2. Simulated spiking response (red) at the output of the Izhikevich neuron during continuous triggering by input pulses (blue).

Fig. 3 shows the enabled frequency tuning behavior. A constant input pulse of $\tau_{in} = 6\,\mu\text{s}$ is applied with an amplitude of $V_{in} = 300\,\text{mV}$. The tuning voltage V_c is swept twice each time in a time window of $\tau_c = 3\,\mu\text{s}$ in the range of up to $V_c = 400\,\text{mV}$ and V_d for also $\tau_d = 6\,\mu\text{s}$ in the range of up to $V_d = 1\,\text{V}$. The maximum frequency achieved for the output spikes is $f_{spike} = 42\,\text{MHz}$. Fig. 3 shows continuous variation of the spiking frequency versus a sweep of the tuning voltage.

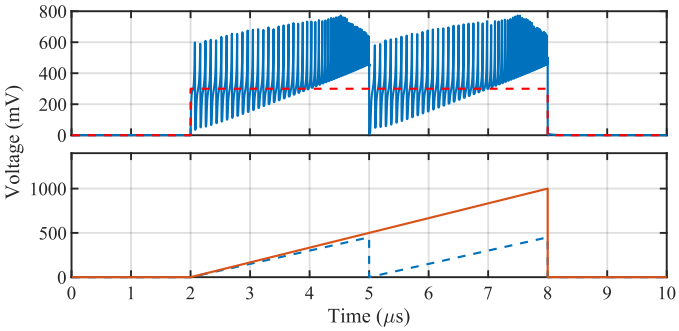

Fig. 3. Simulated adaptive frequency response (blue) with continuous input pulse (red) and sweeping of the tuning voltages V_d (orange) and V_c (blue).

In Fig. 4, the spiking behavior is simulated under the same conditions as in Fig. 2, but now for different spiking times and temperatures. The simulation is performed for the temperatures $T = -40\,^\circ\text{C}; 25\,^\circ\text{C}; 125\,^\circ\text{C}$, to cover the automotive temperature range [8]. As seen in Fig. 4, the circuit operates reliably for each of the simulated temperatures. The spiking behavior is comparable in all three cases. Only the amplitude of the signals differs within an acceptable range depending on the ambient temperature. Compared to the reference temperature of $T = 25\,^\circ\text{C}$, the amplitude of $V_{spike_{25}} = 695\,\text{mV}$ increases to a value of $V_{spike_{-40}} = 897\,\text{mV}$ at a temperature of $T = -40\,^\circ\text{C}$, which corresponds to an amplitude change of about 29%. At a high temperature of $T = 125\,^\circ\text{C}$, compared to the reference temperature, the amplitude decreases to $V_{spike_{125}} = 521\,\text{mV}$, corresponding to a reduction of about 25%. If an appropriate threshold is applied to detect the spikes, the height of spikes is sufficiently high to assume neuron's functionality over the entire temperature range.

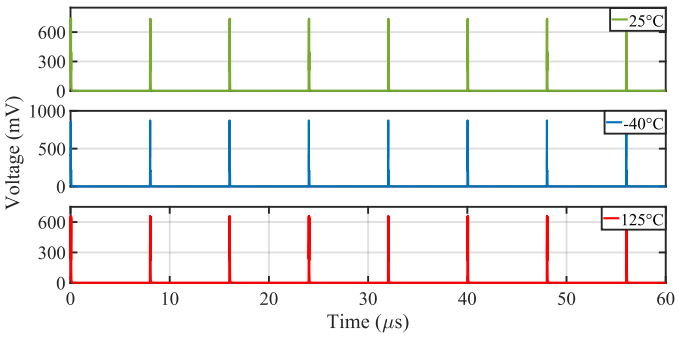

Fig. 4. Simulated comparison of the spike behavior between the reference temperature with $T = 25\,^\circ\text{C}$ and the two temperature extremes for automotive applications of $T = -40\,^\circ\text{C}$ and $T = 125\,^\circ\text{C}$.

B. Logic Gate Configuration

Construction of logic gates using SNN is straightforward, since it is a simple linear and separable problem. The focus in

this work is not to compare the SNN-base logic gates with the conventional CMOS logic, but rather to test applicability of the proposed neuron in a network configuration for possible automotive applications. A description of the two network configurations and the associated encoding procedure is provided in the following.

1) OR-Gate: The information from a spiking neural network can be decoded in two ways - rate coding and temporal coding. Rate coding can be implemented as counting the number of spikes in a certain time frame and interpreting them accordingly. The temporal coding also records the number of spikes in a certain time frame, but additionally the time points carry information. The temporal distance between the individual spikes serves to encode the data. For the following network configuration, rate coding is used, as this is a practical, fast method to interpret correctly the information of the network in this case. The implementation of an OR gate with spiking neurons is shown in Fig. 5. For this purpose, two input neurons (N_1, N_2) are used in each case, which form the input of a possible precedent system. These are driven at a certain input frequency f_{in}. These inputs can be driven externally or from the output of another logical, rate-coded gate. The output signals from the input neurons are fed directly to the output neuron (N_3), synaptic weights are not essential in this configuration.

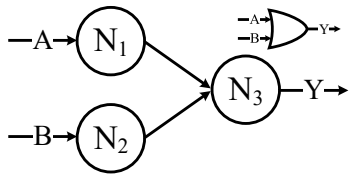

Fig. 5. Network configuration for the OR gate.

The neurons are parameterized in such a way that each input signal leads to an output spike and, in the case of the output neuron, each input spike also leads to an output spike. The coding operates as follows: each input signal with a frequency of $f_{\text{in}} = 125\,\text{kHz}$ is interpreted as a logical "zero". Every input signal with a frequency of $f_{\text{in}} = 250\,\text{kHz}$ represents a logical "one". To satisfy the truth table of a logical OR gate, summarized in Table I, the frequency with which the output neuron spiked is taken as the basis for interpreting the functionality. If it spikes with a frequency of $f_{\text{out}} = 125\,\text{kHz}$, it corresponds to a a logical "zero", but if it responds with spikes with a frequency of $f_{\text{out}} = 250\,\text{kHz}$, these can be interpreted as a logical "one".

TABLE I
TRUTH TABLE FOR AN OR-GATE

A	f_A(kHz)	B	f_B(kHz)	Y	f_Y(kHz)
0	125	0	125	0	125
0	125	1	250	1	250
1	250	0	125	1	250
1	250	1	250	1	250

Fig. 6 demonstrates the simulation of the possible cases of a logical operation of an OR gate. If the input signals A and B correspond to a logical "zero", the output neuron responds with the output signal $Y = 0$, i.e. it spikes at a frequency of 125 kHz. If one of the two inputs changes to a logical "one", the response of the neuron changes to $Y = 1$, i.e. it spikes at a frequency of 250 kHz, in each case. The same case occurs if a logical "one" is present at both inputs. Thus, the truth table in Table I is fulfilled and the correct function of an OR gate is established.

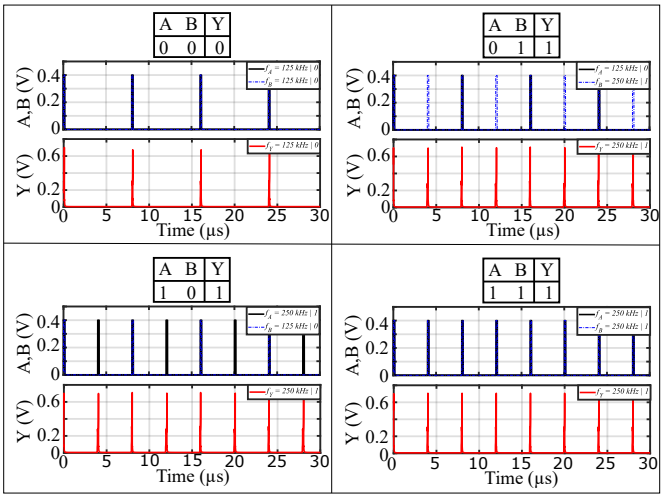

Fig. 6. Simulation of the rate-encoded spiking neural network realizing the function of an OR gate. The signals A (black) and B (blue) represent the respective input signals at the input neurons N_1 and N_2. The output spikes are represented by Y (red).

2) AND-Gate: The AND gate, similarly to the OR gate, is constructed from three neurons, two input neurons (N_1 and N_2) and one output neuron (N_3). However, producing the functionality of a logical AND operation is not as straightforward as in the case of an OR gate. In order for the network to be encoded in the same way, synaptic weights must be introduced in this case. However, since these do not require the ability to change, as in most other applications of SNNs, these can realized by using two resistors to regulate the input current into the output neuron. The network configuration is shown in Fig. 7.

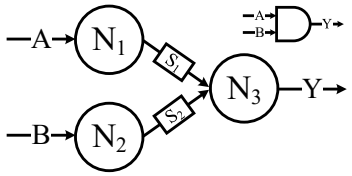

Fig. 7. Network configuration for the AND-Gate, synaptic weights are represented by resistors.

The coding is done in the same way as with the OR Gate. In order to ensure the functionality of the network and to fulfill the truth table II, the weights or sizes of the resistors are chosen in such a way that only a complete excitation of the output neuron can occur when the two input neurons fire simultaneously. If only a single spike arrives at the output

neuron, the membrane capacitor cannot be fully charged, so that no spiking behaviour of the neuron should occur.

TABLE II
TRUTH TABLE FOR AN AND-GATE

A	f_A(kHz)	B	f_B(kHz)	Y	f_Y(kHz)
0	125	0	125	0	125
0	125	1	250	0	125
1	250	0	125	0	125
1	250	1	250	1	250

The simulation results of the AND gate are shown in Fig. 8. If there is a logical "zero" at each of the two inputs (A and B), the output neuron responds with $Y = 0$. If a logical "one" is present at each of the two inputs, the output neuron responds with $Y = 1$. If a logical "zero" and a logical "one" are applied to each of the inputs, the response can also be interpreted as a logical "zero". However, it should be noted here that "intermediate excitations" of the output neuron occur due to the respective intermediate frequency of the logic "one". This can be attributed to the fact that in the neuron model used here, the membrane capacitor potential is equal to the spike potential, so they are not separated from each other. In other words, the input directly mirrors the output, so that while the neuron is not fully excited and does not produce a proper spike, it does receive a small excitation of the membrane capacitor, but this remains below the set threshold voltage. If one uses this configuration further to build more complex structures, these "intermediate excitations" do not pose a problem, as they are filtered out by the next weighting at the latest. Thus, the truth table in Table II is fulfilled and the logical operation of the AND gate is established.

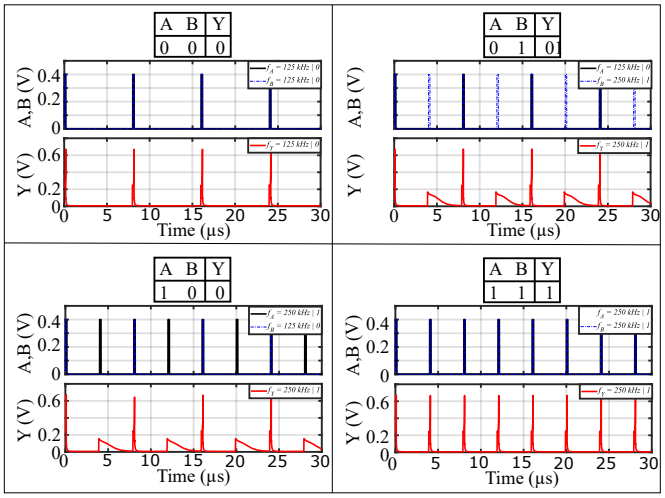

Fig. 8. Simulation of the rate-encoded spiking neural network realizing function of an AND gate. The signals A (black) and B (blue) represent the respective input signals at the input neurons N_1 and N_2. The output spikes are represented by Y (red).

III. MEASUREMENT RESULTS

Fig. 9 shows two sections of the manufactured chip. In (a) the chip section is shown with the modified Izhikevich neuron, the circuit consumes an area of $28\,\mu\text{m} \times 31.5\,\mu\text{m}$. In (b) the chip section is shown with the two logic gates. The OR gate consumes an area of $69\,\mu\text{m} \times 75\,\mu\text{m}$ and the AND gate consumes an area of $80\,\mu\text{m} \times 80\,\mu\text{m}$. It should be noted that the chip area of the test chip is limited only by the pads. Considerable chip area reduction is possible when more neurons are interconnected and driven by an internal source.

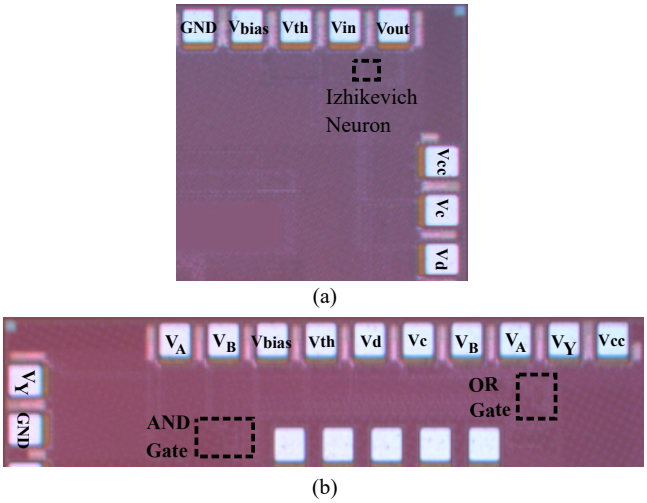

Fig. 9. (a) chip photo section of the modified Izhikevich neuron ($28\,\mu\text{m} \times 31.5\,\mu\text{m}$), b) chip photo section of the OR ($69\,\mu\text{m} \times 75\,\mu\text{m}$) and AND gate ($80\,\mu\text{m} \times 80\,\mu\text{m}$).

A buffer, realized as a simple PMOS stage in a source-follower configuration, is inserted between the output of the neuron and the output pad for measurement purposes (not shown in Fig. 1). Measured response of the neuron is shown in Fig. 10. Spiking activity can be detected for all temperature ranges at the correct time. Hence, neuron exhibits a highly robust behavior of the output signal over the temperature range. The circuit fulfills the automotive temperature range requirement. The deviation from the original form of spikes can be attributed to two effects: additional wiring parasitics and capacitive coupling between the wires. This assumption has been confirmed by resimulation and careful modeling of parasitic capacitances. Additionally, Fig. 10 shows the temperature behavior of the neuron for $T = -40\,°\text{C}; 25\,°\text{C}; 125\,°\text{C}$. For a fair comparison, both in simulation and measurement we use the same values of control signals $V_\text{c}, V_\text{d}, V_\text{th}, V_\text{bias}$.

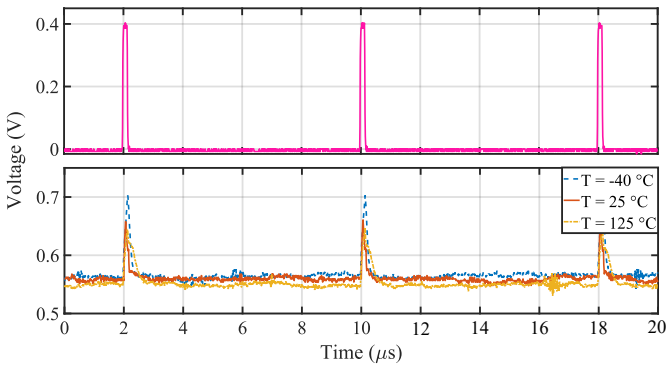

Fig. 10. Measured spiking response of the modified Izhikevich neuron at temperatures $T = -40\,°\text{C}; 25\,°\text{C}; 125\,°\text{C}$.

Figs. 11 and 12 show measurements of the rate-coded SNN-based OR and AND gates shown in Figs. 5 and 7, respectively,

at room temperature. Both circuits operate reliably and fulfill the truth tables described in Tables I and II.

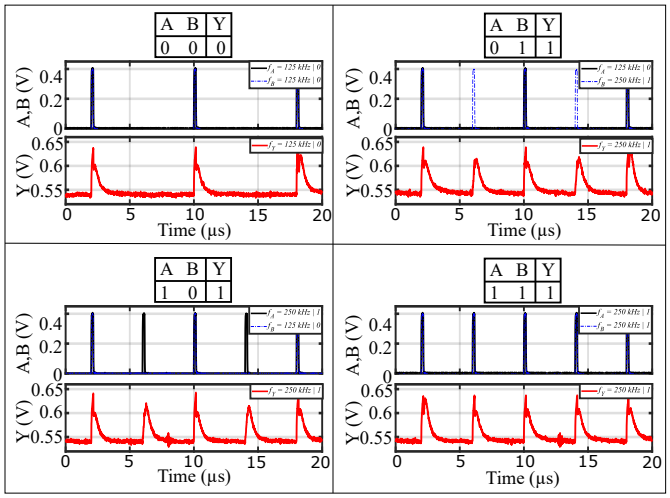

Fig. 11. Measurement of the rate-encoded SNN realizing the function of an OR gate. The signals A (black) and B (blue) represent the input signals at the input neurons N_1 and N_2. The output spikes are represented by Y (red).

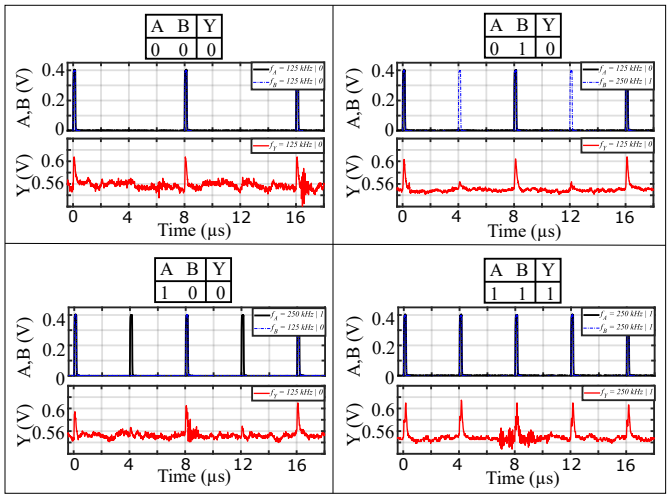

Fig. 12. Measurement of the rate-encoded SNN realizing the function of an AND gate. The signals A (black) and B (blue) represent the input signals at the input neurons N_1 and N_2. The output spikes are represented by Y (red).

Fig. 13 shows measured output signals of OR and AND gates at the two temperature extremes of $-40\,^{\circ}\mathrm{C}$ and $125\,^{\circ}\mathrm{C}$.

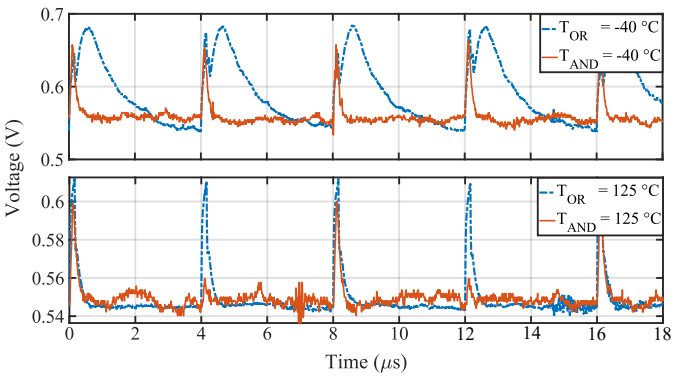

Fig. 13. Measured output signals of AND and OR SNN for the temperature extremes of $-40\,^{\circ}\mathrm{C}$ and $125\,^{\circ}\mathrm{C}$.

It can be noticed clearly that the networks show spiking activity when it is expected in each case for the respective scenarios. However, the amplitudes change slightly as expected in the temperature simulation in Fig. 4. Additionally, the discharge profile of OR gate gets sharper at a high temperature.

IV. Conclusion

This paper presents the first study of neural circuits with respect to their temperature robustness for automotive applications. It is demonstrated that both the single neuron and two network configurations work reliably over the entire temperature range. Modification of the Izhikevich neuron is shown to enable broadband frequency tuning over the tuning voltages. Additionally, we demonstrate a way to implement OR and AND logic gates using rate coding in analog spiking neural networks. Future work can build on these findings, making the use of spiking neural networks tangible for automotive applications.

Acknowledgment

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References

[1] J. Vreeken, "Spiking Neural Networks, an Introduction," Tech. Report UU-CS-2003008, 2003.

[2] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic Electronic Circuits for Building Autonomous Cognitive Systems," *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1388, 2014.

[3] S. Ghosh-Dastidar and H. Adeli, "Spiking neural networks," *International journal of neural systems*, vol. 19, no. 4, pp. 295–308, 2009.

[4] E. M. Izhikevich, "Simple model of spiking neurons," *IEEE transactions on neural networks*, vol. 14, no. 6, pp. 1569–1572, 2003.

[5] A. Tahtirvanci, A. Durdu, and B. Yilmaz, "Classification of EEG signals using spiking neural networks," in *2018 26th Signal Processing and Communications Applications Conference (SIU)*. IEEE, 02.05.2018 - 05.05.2018, pp. 1–4.

[6] M. Arsalan, M. Chmurski, A. Santra, M. El-Masry, R. Weigel, and V. Issakov, "Resource Efficient Gesture Sensing Based on FMCW Radar using Spiking Neural Networks," in *International Microwave Symposium*. IEEE, 2021, pp. 1–4.

[7] B. Wu, Z. Duan, D. Pan, Y. Wang, and Y. Zhou, "A High-linearity CMOS Analog Baseband Circuit with reconfigurable Gain and Bandwidth for 76-81GHz Automotive Radar," in *2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*. IEEE, 31.10.2018 - 03.11.2018, pp. 1–3.

[8] Automotive Electronics Council, Component Technical Committee, "AEC-Q100-012: Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems," released Sept. 14, 2006.

[9] J. Enriquez-Gaytan, F. Gomez-Castaneda, J. A. Moreno-Cadenas, and L. M. Flores-Nava, "Experimental Spiking Neural Network: Solving the XOR Paradigm with Metaheuristics," in *2018 15th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)*. IEEE, 05.09.2018 - 07.09.2018, pp. 1–5.

[10] M. Reljan-Delaney and J. Wall, "Solving the linearly inseparable XOR problem with spiking neural networks," in *2017 Computing Conference*. IEEE, 18.07.2017 - 20.07.2017, pp. 701–705.

[11] J. H. B. Wijekoon and P. Dudek, "Compact silicon neuron circuit with spiking and bursting behaviour," *Neural networks : the official journal of the International Neural Network Society*, vol. 21, no. 2-3, pp. 524–534, 2008.

[12] V. Issakov, A. Bilato, V. Kurz, D. Englisch, and A. Geiselbrechtinger, "A Highly Integrated D-Band Multi-Channel Transceiver Chip for Radar Applications," in *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*. IEEE, 03.11.2019 - 06.11.2019, pp. 1–4.

[13] V. Lammert, S. Achatz, R. Weigel, and V. Issakov, "A 122 GHz ISM-Band FMCW Radar Transceiver," in *2020 German Microwave Conference (GeMiC), IEEE*, March 9-11, 2020.

[14] P. Chevalier, W. Liebl, H. Rucker, A. Gauthier, D. Manger, B. Heinemann, G. Avenier, and J. Bock, "SiGe BiCMOS Current Status and Future Trends in Europe," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*. IEEE, 15.10.2018 - 17.10.2018, pp. 64–71.